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Design and operation of DSTATCOM for power quality improvement in distribution systems

Manish Kumar, Anil Swarnkar, Nikhil Gupta, Khaleequr Rehman Niazi

Department of Electrical Engineering, Malaviya National Institute of Technology, Jaipur, Rajasthan, India
E-mail: manishkumar6462@gmail.com

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Abstract: This study provides a control scheme for distribution static compensator (DSTATCOM) which compensates three-phase, four-wire distribution system and operates the DSTATCOM in voltage control mode (VCM). This algorithm provides achievement of advantages of current control mode operation while DSTATCOM operated in VCM. Compensator injects reactive and harmonic component of load current and it provides fast voltage regulation at the load terminal with maintaining nearly unity power factor (UPF). Deadbeat voltage control law is used for generating switching pulses for insulated gate bipolar transistor (IGBT) switches and reference terminal voltage is generated by system in such a way that point of common coupling maintains nearly UPF. The proposed design is implemented to mitigate power quality issues induced by source as well as load and it is found to be efficient and robust which is validated through performance under nominal operation, unbalance and distorted source voltage, sag-swell and unbalancing in load for any types of load. Capability of this arrangement has been verified using result obtained from MATLAB–SIMULINK-based environment. Different types of loads have been considered (balanced and unbalanced, linear and non-linear) to check the performance of this arrangement.

1 Introduction

Modern power consumers are becoming more concerned about the quality of power, which is being supplied to them. The rapid improvements in modern-day consumer electronics are increasing the power quality issues. Alternatively, quick growth of renewable power generation coupled with various power electronic converters further increases the PQ issues in distribution system. The combination of these electronic converters with unbalanced and reactive load deforms the source current; it causes pollution at the load bus [1–3]. The PQ problems generated at the distribution system may be voltage or current related. The voltage related PQ problems such as sag-swell or any unbalancing in source or load voltage it get worse the performance of sensitive load [4]. A compensated distribution system with distribution static compensator (DSTATCOM) is able to mitigate the PQ problems; it is functionally working as shunt active filter which convinces the reactive and harmonic component of load current [5]. In literature, generally, PQ issues either incorporate voltage related issues or current related issues [6–13], but the main challenging work is mitigation of both voltage and current related PQ problems simultaneously. DSATCOM operates in current control mode can mitigate current related PQ problems such as unbalancing in source current, harmonic distortion, and poor power factor but it cannot afford voltage improvement during any voltage disturbance at the load terminal [14].

This paper provides a control scheme which operates the DSTATCOM in voltage control mode (VCM) by getting all the advantages of current control mode (CCM) operation. Fig. 1 shows the three-phase, four-wire distribution system compensated with DSTATCOM. Load terminal where DSTATCOM is connected is called point of common coupling (PCC). A deadbeat voltage control algorithm [15, 16] is used for generating the switching pulse for DSTATCOM, which regulates the terminal voltage at nominal value during any voltage disturbance. To achieve all the advantages of CCM operation, instantaneous symmetrical component theory [17] was used to generate reference terminal voltage, while compensator provides fast voltage regulation and it also injects the reactive and harmonic component of load current. The proposed design is found to be efficient and robust; it is validated through performance under different types of load and unbalancing in source or load side which is explain in detailed simulation results.

2 System configuration

The block diagram of three-phase, four-wire distribution system is shown in Fig. 1. It contains a combination of reactive, unbalance, linear and non-linear load connected with DSTATCOM at PCC. Realisation of DSTATCOM [18] by three-phase voltage source inverter with the two neutrally clamped capacitor acts as a DC voltage source. This configuration provides independent control of switches of each leg in order to control injecting current to achieve its objectives. Voltage across DC capacitor is maintained at a constant level by using closed-loop proportional-integral (PI) controller through interfacing inductance L_f and resistance R_f of voltage source inverter (VSI). A shunt filter capacitor C_{cf} is individually connected for each phase across the terminal to eliminate high switching frequency of harmonic component. Here, R_s and L_s are Thevenin's equivalent resistance and inductance, respectively, present at source side of PCC. $V_{sj,}$ V_{tj}, i_{sj}, i_{lj} and i_{ftj} represent the source voltage, terminal voltage, source current, and injected filter currents to the terminal, respectively, with $j = a, b, c$ as three-phase.

3 Control approach

A single line equivalent diagram of Fig. 1 is shown in Fig. 2. It is used for realising the control strategy of DTATCOM. V_{dc} u is output voltage of VSI depending on control unit u which is either +1 or −1. If u is +1 then VSI supplied to terminal is $+V_{dc}$. It means upper switch of VSI is ON, similarly if u is −1 then VSI output is $-V_{dc}$ that means lower switch is ON. A deadbeat voltage control law is used to regulate the terminal voltage at reference value. Instantaneous symmetrical component theory is used to generate

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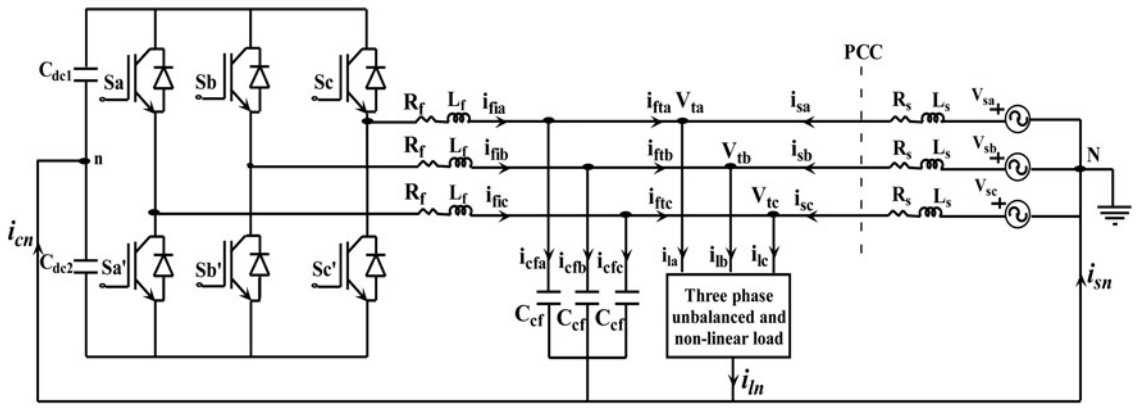

Fig. 1 *Block diagram of the DSTATCOM-compensated distribution system*

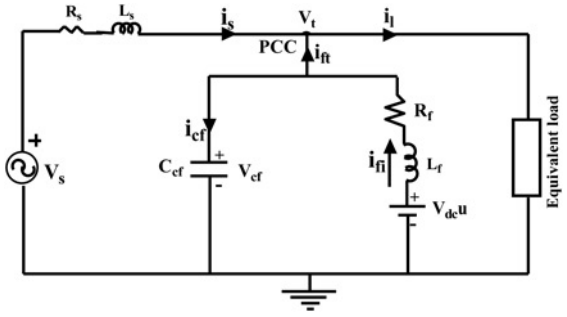

Fig. 2 *Single line equivalent diagram of DSTATCOM-compensated circuit*

reference terminal voltage such that advantages of CCM are achieved at nominal load. For preventing the continuous charging or discharging of DC capacitor, a PI controller is used to regulate it at constant value. The complete block diagram of controller is shown in Fig. 3.

3.1 Deadbeat voltage-control law

For deriving this control law we use state-space equation of circuit shown in Fig. 2. Taking voltage across filter capacitor and injected current as state variables, control unit and injected current to the terminal take as control vector.

The state-space equation in continuous form is given by

$$\dot{x} = Ax(t) + Bz(t) \tag{1}$$

where

$$A = \begin{bmatrix} 0 & \frac{1}{C_{\rm cf}} \\ \frac{-1}{L_{\rm f}} & \frac{-R_{\rm f}}{L_{\rm f}} \end{bmatrix} \quad \text{and} \quad B = \begin{bmatrix} 0 & \frac{-1}{C_{\rm cf}} \\ \frac{V_{\rm dc}}{L_{\rm f}} & 0 \end{bmatrix} \tag{2}$$

$$x = \begin{bmatrix} v_{\rm cf} \\ i_{\rm fi} \end{bmatrix} \quad \text{and} \quad z = \begin{bmatrix} u_{\rm c} \\ i_{\rm ft} \end{bmatrix} \tag{3}$$

The equivalent discrete form of (1) is

$$x(k+1) = Gx(k) + {\rm Hz}(k) \tag{4}$$

where

$$G = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \quad \text{and} \quad H = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} \tag{5}$$

Rewriting the (4) gives

$$v_{\rm cf}(k+1) = G_{11}v_{\rm cf}(k) + G_{12}i_{{\rm f}i}(k) + H_{11}u_{\rm c}(k) + H_{12}i_{\rm ft}(k) \tag{6}$$

The value of G and H is calculated by using simplification; it is obtained from various derivations [17]

$$G = {\rm e}^{AT_d} \quad \text{and} \quad H = \int_0^{T_d} {\rm e}^{At} B \, {\rm d}t \tag{7}$$

where $T_{\rm d}$ is period of sample k at the kth sampling instant. To regulate the terminal voltage at reference value we must choose cost

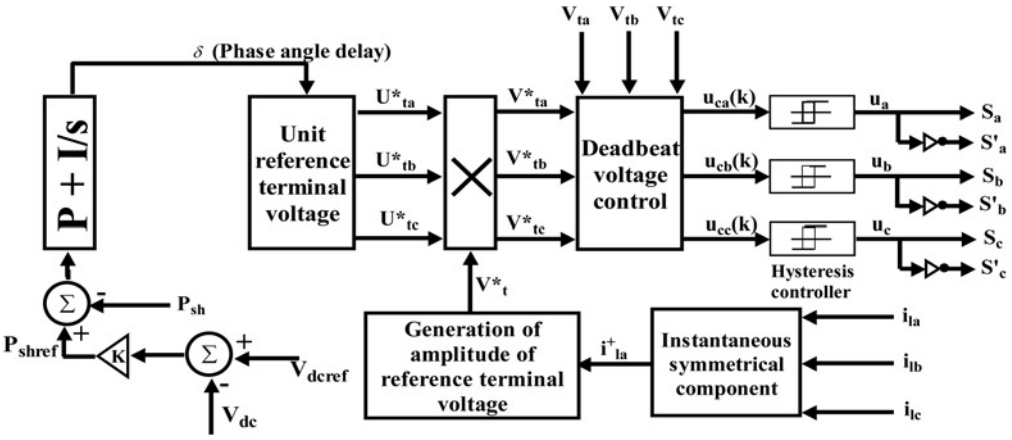

Fig. 3 *Complete block diagram of the controller to generate switching pulse for VSI*

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function (J) such that it minimises the difference between instant value and reference value. Therefore

$$J = \left[v_{\mathrm{cf}}(k+1) - v_{\mathrm{t}}^{*}(k+1)\right]^{2} \tag{8}$$

Here, $v_{\mathrm{t}}^{*}(k+1)$ is reference terminal voltage at $(k+1)$th instant and $v_{\mathrm{cf}}(k+1)$ is voltage of shunt capacitor which is equal to instantaneous terminal voltage at $(k+1)$th instant. To minimise the difference between reference voltage and terminal voltage the cost function with respect to $u(k)$ is differentiated as

$$\frac{\partial J}{\partial u(k)} = 2\left[v_{\mathrm{cf}}(k+1) - v_{\mathrm{t}}^{*}(k+1)\right]\frac{\partial v_{\mathrm{cf}}}{\partial u(k)} = 0 \tag{9}$$

On solving (6) and (9) we get

$$u_{\mathrm{c}}(k) = \frac{v_{\mathrm{t}}^{*}(k+1) - G_{11}v_{cf}(k) - G_{12}i_{2}(k) - H_{12}i_{\mathrm{fl}}(k)}{H_{11}} \tag{10}$$

The value of $u_{\mathrm{c}}(k)$ obtained from (10) provides a deadbeat action, which is used in generation of switching pulse with the help of hysteresis controller on comparing a particular hysteresis band h. The value of G, H and VSC parameters are obtained from various derivations and simplification [19]. By using Lagrange extrapolation formula of second order we can obtain future reference voltage $v_{\mathrm{t}}^{*}(k+1)$ from present state as

$$v_{\mathrm{t}}^{*}(k+1) = 3v_{\mathrm{t}}^{*}(k) - 3v_{\mathrm{t}}^{*}(k-1) + v_{\mathrm{t}}^{*}(k-2) \tag{11}$$

3.2 Generation of reference terminal voltage

Generated reference terminal voltage provides advantages of CCM while DSTATCOM operates in VCM. As only fundamental component of positive sequence of load current (i_{la1}^{+}) is responsible for delivering the active power to the load therefore, assume the reference source current will be equal to it in order to maintain nearly unity power factor (UPF) at the load terminal. Using the symmetrical component theory to obtain zero, positive, and negative sequences of load current from instantaneous load current is given as

$$\begin{bmatrix} i_{\mathrm{la}}^{0}(t) \\ i_{\mathrm{la}}^{+}(t) \\ i_{\mathrm{la}}^{-}(t) \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^{2} \\ 1 & \alpha^{2} & \alpha \end{bmatrix}\begin{bmatrix} i_{\mathrm{la}}(t) \\ i_{\mathrm{lb}}(t) \\ i_{\mathrm{lc}}(t) \end{bmatrix} \tag{12}$$

Fundamental positive sequence of load current is calculated by Fourier analysis of the positive sequence of load current and obtained value can be expressed as

$$I_{\mathrm{la1}}^{+} = \left|I_{\mathrm{la1}}^{+}\right| \angle I_{\mathrm{la1}}^{+} \tag{13}$$

So,

$$i_{\mathrm{la1}}^{+}(t) = \sqrt{2}\left|I_{\mathrm{la1}}^{+}\right| \sin\left(\omega t + \angle I_{\mathrm{la1}}^{+}\right) \tag{14}$$

For UPF at nominal load the fundamental component of positive sequence of load current must be equal to source current. Therefore, reference source current for phase-a is given as

$$i_{\mathrm{sa}}^{*} = i_{\mathrm{la1}}^{+}(t) = \sqrt{2}\left|I_{\mathrm{la1}}^{+}\right| \sin\left(\omega t - \delta_{0}\right) \tag{15}$$

Here δ_{0} is nominal load angle. If we consider the reference terminal voltage as reference phasor, UPF at the terminal for phase a will be

$$V_{\mathrm{ta}}(t) = \sqrt{2}V_{\mathrm{t}}^{*} \sin \omega t \tag{16}$$

$$i_{\mathrm{sa}}^{*} = \sqrt{2}\left|I_{\mathrm{la1}}^{+}\right| \sin \omega t \tag{17}$$

$$V_{\mathrm{sa}}(t) = \sqrt{2}V \sin\left(\omega t + \delta_{0}\right) \tag{18}$$

where V_{t}^{*} and V are RMS values of reference terminal and source voltage, respectively. From Fig. 2 terminal voltage can be calculated for phase-a

$$V_{\mathrm{ta}}(t) = V_{\mathrm{sa}}(t) - L_{\mathrm{s}}\frac{di_{\mathrm{sa}}^{*}}{\mathrm{d}t} - R_{\mathrm{s}}i_{\mathrm{sa}}^{*} \tag{19}$$

From (16) to (19)

$$V_{\mathrm{t}}^{*}\angle 0 = V\angle\delta_{0} - \left(R_{\mathrm{s}} + jX_{\mathrm{s}}\right)\left|I_{\mathrm{la1}}^{+}\right|\angle 0 \tag{20}$$

On simplifying (20) we get

$$V\cos\delta_{0} = V_{\mathrm{t}}^{*} + \left|I_{\mathrm{la1}}^{+}\right|R_{\mathrm{s}} \tag{21}$$

$$V\sin\delta_{0} = \left|I_{\mathrm{la1}}^{+}\right|X_{\mathrm{s}} \tag{22}$$

We can remove the δ_{0} by

$$V^{2} = \left(V_{\mathrm{t}}^{*} + \left|I_{\mathrm{la1}}^{+}\right|R_{\mathrm{s}}\right)^{2} + \left(\left|I_{\mathrm{la1}}^{+}\right|X_{\mathrm{s}}\right)^{2} \tag{23}$$

Thus, we can write the generated reference terminal voltage as

$$V_{\mathrm{ta}}^{*}(t) = \sqrt{2}V_{\mathrm{t}}^{*} \sin\left(\omega t - \delta\right) \tag{24}$$

$$V_{\mathrm{tb}}^{*}(t) = \sqrt{2}V_{\mathrm{t}}^{*} \sin\left(\omega t - \frac{2\pi}{3} - \delta\right) \tag{25}$$

$$V_{\mathrm{tc}}^{*}(t) = \sqrt{2}V_{\mathrm{t}}^{*} \sin\left(\omega t + \frac{2\pi}{3} - \delta\right) \tag{26}$$

3.3 Voltage regulation of capacitor at DC bus

In practice some losses occur in VSI therefore, it continuously discharges the capacitor. For preventing the continuously charging or discharging of capacitor a closed loop PI controller should be used to regulate the voltage of DC capacitor at constant level. This generates a power angle δ and it provides a phase angle delay to the reference terminal voltage in such a way the total average power entering at terminal (P_{sh}) equals to sum of average power required to load (P_{load}) and losses occur in DSTATCOM (P_{loss}). Thus, in power balance condition the average real power at the terminal will be

$$P_{\mathrm{sh}} = P_{\mathrm{load}} + P_{\mathrm{loss}} \tag{27}$$

4 Simulation results

This section provides a detailed simulation results under different cases to investigate the performance of DSTATCOM.

To validate the performance of DSTATCOM cases considered as: performance under nominal load, unbalance and distorted source voltage, sag-swell, sudden load interrupt. Required harmonic components are delivered by All Simulink parameters, which are used and presented in Table 1.

Table 1 Parameters used in simulation

system voltage: 360 V (peak)
terminal bus voltage: 300 V (peak), sinusoidal balanced
feeder impedance: $1+j3.14\ \Omega$
linear load: $Z_a=40\ \Omega$, $Z_b=50\ \Omega$, $Z_c=72+j84\ \Omega$
non-linear load: three-phase rectifier with R–L load of $50+j62.8\ \Omega$
DC capacitors (C_1, C_2): 2200 μF each
interface inductors (L_f, R_f): 20 mH, 0.2 Ω
|AC capacitors (C_{cf}): 50 μF in each phase
voltage controller gains of DC capacitor loops: $K=10$
δ control loop gains: $P=11e{-}6$, $I=9e{-}6$
reference value of total DC capacitor voltage: 1200 V
control signal hysteresis band for each phase: $h=1$

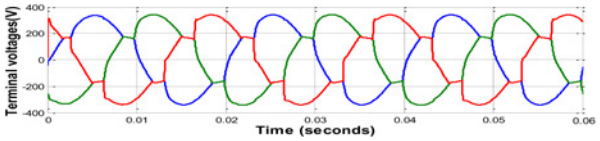

Fig. 4 *Before compensation terminal voltages*

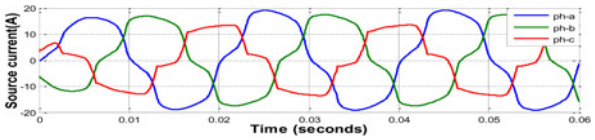

Fig. 5 *Before compensation source currents*

4.1 Performance under nominal operation

Due to the presence of combination of reactive, unbalance, linear and non-linear load source current get distorted and unbalanced. Distorted source current flow through feeder impedance; it also distorts the terminal voltages as shown in Figs. 4 and 5. Here, total harmonic distortion (THD) level present in source current and terminal voltage is nearly 15% and 12%, respectively, which is unacceptable for IEEE standard and it should be <5%. Figs. 6 and 7 show the compensated terminal voltages and source current, respectively. Here we can observe that the terminal voltage is regulated at constant value with sinusoidal and source current becomes balanced.

After compensation the THD level present the source current and terminal voltage are nearly 3% and 2%, respectively. To regulate terminal voltage at constant value the compensator injects reactive and harmonics component of load current as shown in Fig. 8.

Here we can observe that source current becomes sinusoidal while load current remains distorted, it means that the reactive and harmonic component required to the load is delivered by compensator.

4.2 Performance under unbalanced and distorted source voltage

In case of unbalance and distorted source voltage DSTATCOM can able to regulate the terminal voltage at constant level with cleanup all disturbances. To confirm that this source voltage taken is unbalanced and to make it distorted third harmonics is introduced as

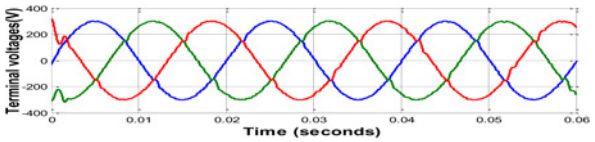

Fig. 6 *After compensation terminal voltages*

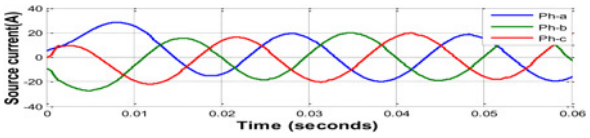

Fig. 7 *After compensation source currents*

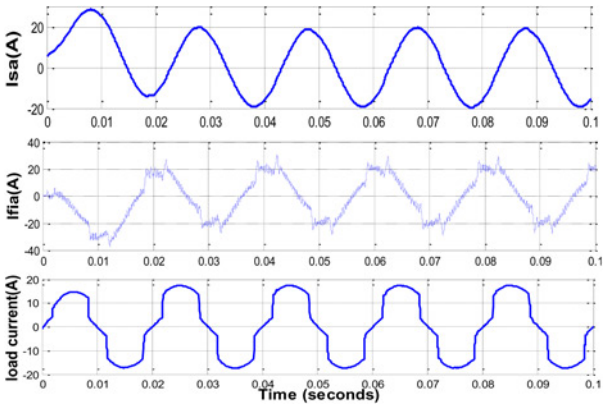

Fig. 8 *Source current, injected current and load current*

Phase-a: 360 V (peak) and 20% third harmonics.
Phase-b: 400 V (peak) and 15% third harmonics.
Phase-c: 300 V (peak) and 10% third harmonic.

The load parameters are used for above condition are given in Table 1. Unbalance source voltage with harmonics as above given parameters is shown in Fig. 9. When compensator is connected to the system at time 0.03 s it regulates the terminal voltage at 300 V and makes it balanced and sinusoidal as shown in Fig. 10. THD level at the terminal voltage is also reduced after

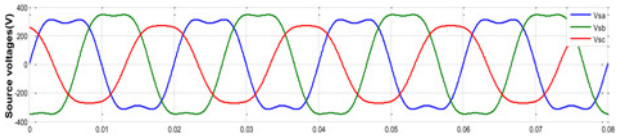

Fig. 9 *Unbalanced source voltage with harmonics*

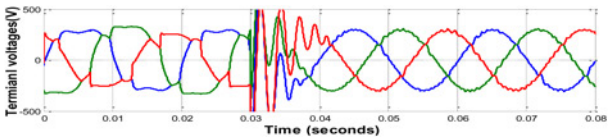

Fig. 10 *Terminal voltages before and after compensation*

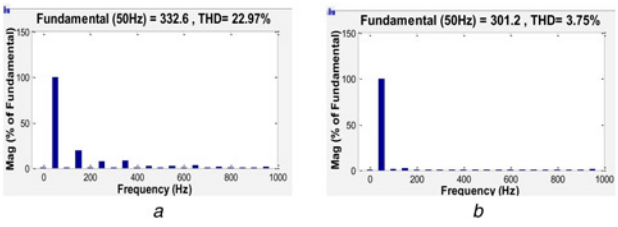

Fig. 11 *Harmonic spectrum in terminal voltage*
a Before compensation
b After compensation

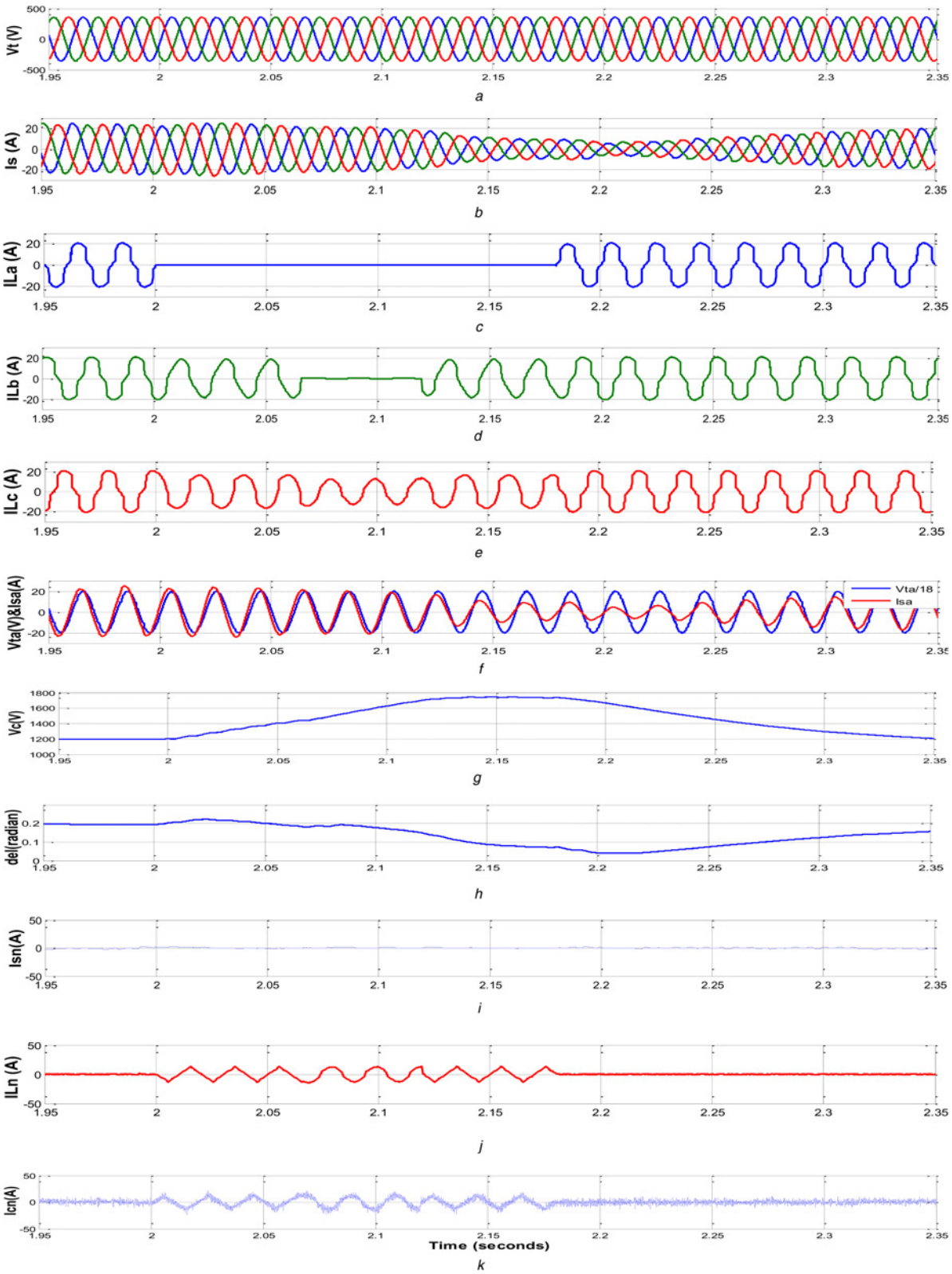

Fig. 12 *Performance of DSTATCOM with non-linear load with unbalancing*
a Terminal voltages
b Source currents
c Load current phase a
d Load current phase b
e Load currents phase c
f Phase difference between voltage and current waveform of phase a
g DC bus voltage
h Load angle
i Source neutral current
j Load neutral current
k Neutral current supplied by compensator

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compensation. Fig. 11 shows the harmonic spectrum of terminal voltage before and after regulations for phase-a; it can be seen that the THD in terminal voltage reduced up to 3.75%. The THD in phase-b and phase-c after compensation is also reduced to 3.96 and 4.53%, respectively.

4.3 *Performance under sudden load interrupt*

Due to unbalancing in load a high amount of current flow through the neutral wire which may cause insulation failure of neutral wire and other consequences. To investigate the performance of DSTATCOM under unbalanced load condition convert the three-phase load into two-phase load at time 2.0 s and to single-phase at 2.06 s and loads are reapplied from single-phase to two-phase at 2.12 s and three-phase at 2.18 s as shown in Fig. 7. Here we can observe the source current is balanced and sinusoidal while load current is unbalanced. The source side neutral current maintained nearly zero and neutral current required to the load is compensated by compensator which is shown in Figs. 12*i–k*, respectively. Fig. 12*a* shows the terminal voltage regulated at nominal value. Terminal voltage and source current nearly in same phase is shown in Fig. 12*f* it means maximum amount of reactive power required by the load is compensated by compensator. The closed-loop PI controller generates the load angle (δ) which is settled around 0.195 radian or 11.17°. When capacitor voltage increases the load angle decreases and when it decreases the load angle increases in order to maintain DC bus voltage at constant value 1200 V. The loads are taken linear load $R = 40\ \Omega$ in each phase and non-linear load as three-phase bridge rectifier with *R–L* load of $50 + j62.8\ \Omega$.

5 Conclusion

This paper concludes the PQ issues of distribution system. To provide safe and clean power required at the distribution bus a DSTATCOM is used. There present a designed controller which operates the DSTATCOM in VCM by achieving the advantages of CCM operation. The SIMULINK results obtained on MATLAB platform show the following key points: (i) to make terminal voltage and source current balanced, sinusoidal and distortion-less the compensator provide reactive and harmonic component to the load current; (ii) it regulates the terminal voltage at nominal value; (iii) it provides fast voltage regulation in case sudden load interrupt with maintaining nearly UPF and it also compensates the neutral current required to the load in order to make source current balance; and (iv) it can be able to provide balanced and distortion-less voltage at the distribution bus in case of unbalanced and distorted source voltage.

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